CLAIMS:

What is claimed is:

1. A device coupled to a serial communications bus, comprising:

a main section;

address logic;

switches;

switch logic for controlling a current position of said switches coupled to said switch logic;

said switches being coupled to said communications bus; and

said switches controlling whether said main section, said address logic, said switch logic, or a combination of said main section, address logic, and switch logic is currently coupled to said communications bus.

2. The device according to claim 1, further comprising:

said device being an I^2C device.

3. The device according to claim 1, further comprising:

said communications bus having only a clock signal line and a data signal line.

4. The device according to claim 1, further comprising:

said main section being coupled to said communications bus through said switches.

5. The device according to claim 1, further comprising:

said main section, said address logic, and said switch logic being logically removed from said communications bus when said switches are in a first position.

6. The device according to claim 1, further comprising:

said main section being logically removed from said communications bus when said switches are in a second position; and

said address logic and said switch logic remaining logically connected to said communications bus when said switches are in a second position.

7. The device according to claim 1, further comprising:

said main section, said address logic, and said switch logic being logically connected to said communications bus when said switches are in a third position.

8. The device according to claim 1, further comprising:

said switches including an input switch device and an output switch device.

9. The device according to claim 8, further comprising:

said communications bus having only a clock signal line and a data signal line;

said input switch device being a double pole rotary switch having a first pole coupled to said data signal

line and a second pole coupled to said clock signal line; and

said output switch device being a double pole rotary switch having a first pole coupled to said data signal line and a second pole coupled to said clock signal line.

10. The device according to claim 1, further comprising:

at least one second device coupled to said communications bus after said device;

said switches including an input switch device and an output switch device;

said main section, said address logic, and said switch logic being logically connected to said communications bus when said output switch device is in a fourth position; and

said at least one second device being logically removed from said communication bus when said output switch device is in said fourth position.

11. The device according to claim 1, further comprising:

at least one second device coupled to said communications bus after said device;

said switches including an input switch device and an output switch device;

said main section, said address logic, and said switch logic being logically removed from said communications bus when said input switch device is in a fourth position; and

said at least one second device being logically removed from said communication bus when said input switch device is in said fourth position.

12. The device according to claim 1, further comprising:

said address logic for storing an address for said device, said device being addressed on said communications bus utilizing said address.

13. The device according to claim 12, further comprising:

said device having a hardwired address; and

said address stored in said address logic overriding at least a portion of said hardwired address.

14. A method for utilizing a device coupled to a serial communications bus, comprising:

said device including a main section, address logic, switches, and switch logic;

coupling said device to said communications bus utilizing said switches;

controlling a current position of said switches utilizing said switch logic;

controlling whether said main section, said address logic, said switch logic, or a combination of said main section, address logic, and switch logic is currently coupled to said communications bus utilizing said switch logic.

15. The method according to claim 14, further comprising:

said communications bus having only a clock signal line and a data signal line.

16. The method according to claim 14, further comprising:

logically removing said main section, said address logic, and said switch logic from said communications bus when said switches are in a first position.

17. The method according to claim 14, further comprising:

logically removing said main section from said communications bus when said switches are in a second position; and

logically connecting said address logic and said switch logic remaining to said communications bus when said switches are in a second position.

18. The method according to claim 14, further comprising:

logically connecting said main section, said address logic, and said switch logic to said communications bus when said switches are in a third position.

19. The method according to claim 14, further comprising:

said switches including an input switch device and an output switch device.

20. The method according to claim 19, further comprising:

said communications bus having only a clock signal line and a data signal line;

said input switch device being a double pole rotary switch;

coupling a first pole of said input switch device to said data signal line and a second pole of said input switch device to said clock signal line;

said output switch device being a double pole rotary switch; and

coupling a first pole of said output switch device to said data signal line and a second pole of said output switch device to said clock signal line.

21. The method according to claim 14, further comprising:

coupling at least one second device to said communications bus after said device;

said switches including an input switch device and an output switch device;

logically connecting said main section, said address logic, and said switch logic to said communications bus when said output switch device is in a fourth position; and

logically removing said at least one second device from said communication bus when said output switch device is in said fourth position.

22. The method according to claim 14, further comprising:

coupling at least one second device to said communications bus after said device;

said switches including an input switch device and an output switch device;

logically removing said main section, said address logic, and said switch logic from said communications bus when said input switch device is in a fourth position; and

logically removing said at least one second device from said communication bus when said input switch device is in said fourth position.

23. The method according to claim 14, further comprising:

storing an address in said address logic for said device; and

addressing said device on said communications bus utilizing said stored address.

24. The method according to claim 14, further comprising:

said device having a hardwired address; and

overriding at least a portion of said hardwired address using said address stored in said address logic.

25. The method according to claim 14, further comprising:

coupling a plurality of devices to said communication bus;

determining whether any of said plurality of devices are addressed utilizing a duplicate address;

in response to determining that at least two of said plurality of devices are addressed utilizing said duplicate address, sending a command to said at least two of said plurality of devices to remove all of said plurality of devices that are downstream from said at least two of said plurality of devices from said communications bus;

storing a first new address in address logic included in a first one of said at least two of said plurality of devices;

sending a command to said plurality of devices to logically connect said plurality of devices to said communications bus.

26. The method according to claim 14, further comprising:

coupling a plurality of devices to said communication bus;

determining whether an address of one of said plurality of devices is to be changed;

in response to determining that said address of said one of said plurality of devices is to be changed, storing a new address in address logic included in said one of said plurality of devices; and

addressing said one of said plurality of devices utilizing said new address.

27. An I^2C device coupled to an I^2C serial communications bus having only a clock signal line and a data signal line, said I^2C device comprising:

a main section;

address logic;

switches connected to said communications bus;

switch logic for controlling a current position of said switches coupled to said switch logic;

said switches controlling whether said main section, said address logic, said switch logic, or a combination of said main section, address logic, and switch logic is currently coupled to said communications bus;

said main section, said address logic, and said switch logic being logically removed from said communications bus when said switches are in a first position;

said main section being logically removed from said communications bus when said switches are in a second position;

said address logic and said switch logic remaining logically connected to said communications bus when said switches are in a second position;

said main section, said address logic, and said switch logic being logically connected to said communications bus when said switches are in a third position;

said switches including an input switch device and an output switch device;

said input switch device being a double pole rotary switch having a first pole coupled to said data signal line and a second pole coupled to said clock signal line;

said output switch device being a double pole rotary switch having a first pole coupled to said data signal line and a second pole coupled to said clock signal line;

at least one second device coupled to said communications bus after said device;

said main section, said address logic, and said switch logic being logically connected to said communications bus when said output switch device is in a fourth position;

said at least one second device being logically removed from said communication bus when said output switch device is in said fourth position;

said main section, said address logic, and said switch logic being logically removed from said communications bus when said input switch device is in a fourth position;

said at least one second device being logically removed from said communication bus when said input switch device is in said fourth position;

said address logic for storing an address for said device, said device being addressed on said communications bus utilizing said address;

said device having a hardwired address; and

said address stored in said address logic overriding at least a portion of said hardwired address.